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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,060	09/30/2003	Xiangfeng Duan	2132.0010002	1190

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STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,060	DUAN ET AL.	
	Examiner	Art Unit	
	Igwe U. Anya	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *173-233* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *173-233* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 173, 174, 179, 181, 182, 186, 201, 203, 207, 214, and 223 are rejected under 35 U.S.C. 102(e) as being anticipated by Eaton et al. (US Patent 6760245).

3. Eaton et al. teach an electronic substrate (12) having a plurality of semiconductor devices (fig. 3), comprising a substrate, a thin film of nanowires (42, 44), formed on said substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions, and contacts formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices (col. 4 lines 8 – 50);

wherein at least a subset of the semiconductor devices comprises transistors (fig. 3), the contacts comprise gate (20), source and drain electrodes formed above or below said thin film of nanowires, wherein said thin film of nanowires forms channels between said source and said drain electrodes (col. 4 lines 8 – 50);

wherein at least a subset of the semiconductor devices comprises memory devices (col. 1 lines 29 – col. 2 line 23);

wherein the nanowires are aligned parallel to their long axis, the nanowires are aligned parallel to an axis between the source and drain electrodes, the gate, source and drain electrodes are formed in the nanowires, a subset of the semiconductor devices is electrically coupled to another circuit and at least one channel of said channels, a first end of at least two nanowires of said nanowires is electrically coupled with a first contact of said channel, and a second end of said at least two nanowires is electrically coupled with a second contact of said channel (col. 4 lines 8 – 50); and

wherein the circuit is a memory circuit (col. 3 line 46 – col.4 line 7).

4. Claims 173 – 176, 185, 192, 195, 224 – 233 are rejected under 35 U.S.C. 102(e) as being anticipated by Avouris et al. (USPAP 2004/0061422).

5. Avouris et al. teach a method of making an electronic substrate having a plurality of semiconductor devices, comprising:

(a) forming on a substrate (102) a thin film of nanowires (103) with a sufficient density of nanowires to achieve an operational current level;

(b) defining a plurality of semiconductor device regions in the thin film of nanowires; and

(c) forming contacts (104, 105) at the semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices.

further comprising aligning the nanowires substantially parallel to their long axis (Fig. 1A).

wherein step (c) comprises forming source and drain electrodes, whereby the nanowires form a channel having a length between respective ones of the source and drain electrodes (paragraph 32).

further comprising a step of forming gate electrodes (101).

wherein step (c) comprises forming anode and cathode electrodes (figs.1);

wherein the nanowires (103) are aligned parallel to an axis between the source(104) and drain (105) contacts (figs. 1);

wherein the gate, source and drain electrodes are formed on the substrate, and the thin film of nanowires are formed on the gate, source and drain electrodes (fig. 1B).

wherein said thin film of nanowires forms a p-n junction between said anode and cathode electrodes (paragraph 37);

wherein said thin film of nanowires comprises a sufficient number of nanowires to have an on state current level in the channels of greater than 10 nanoamps. (paragraph 39); and

wherein at least a subset of the channels comprises a p-n junction, whereby during operation the p-n junctions emit light (paragraph 36).

6. Claims 173, 174, 183 – 184, 193, 194, and 200 are rejected under 35 U.S.C. 102(e) as being anticipated by Lieber et al. (USPAP 2002/0117659).

7. Lieber et al. teach an electronic substrate having a plurality of semiconductor devices, comprising a substrate, a thin film of nanowires, formed on said substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions, and contacts

formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices (paragraphs 132 – 136, & fig 1);

wherein the channels comprise more than one nanowire, and a subset of the gate electrodes comprise more than one thin film of nanowires (paragraph 143, & fig. 1B);

wherein at least a subset of said nanowires are oxidized to thereby form a gate dielectric (paragraph 158, & figs. 16A, 16B);

wherein the gate electrodes are formed on the substrate, the thin film of nanowires is formed on the gate electrodes, and the source and drain electrodes are formed on the thin film of nanowires (1A);

wherein the source and drain electrodes are formed on the substrate, the thin film of nanowires is formed on the source and drain electrodes, and the gate electrodes are formed on the thin film of nanowires (fig. 4A); and

wherein the gate, source and drain electrodes are formed on the thin film of nanowires (16A)

8. Claims 173, 178, 197 – 199, 201, 202, 205, 206, 218, 220 and 222 are rejected under 35 U.S.C. 102(e) as being anticipated by Majumdar et al. (USPAP 2002/0175408).

9. Majumdar et al. teach an electronic substrate having a plurality of semiconductor devices, comprising a substrate, a thin film of nanowires, formed on said substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions, and contacts

formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices (paragraph 168, & fig. 31);

wherein at least a subset of the nanowires have doped cores, doped cores and shells (paragraphs 71 – 79, & figs. 2 –11);

wherein at least a subset of the semiconductor devices are physically coupling to another circuit (paragraph 237);

wherein said nanowires are ballistic conductors having a mobility greater than that of single crystal semiconductor material (paragraph 226);

wherein the circuit is a logic circuit (paragraph 226);

wherein said nanowires are a formed as a monolayer film, a sub monolayer film, or a multi layer film (paragraph 101); and

wherein said nanowires comprise sufficient density to have statistic probability of achieving a device anywhere on the substrate (paragraph 166)

10. Claims 173, 180, 187 – 190, 196, 201, 204, 205, 208, 215 – 217, and 219 are rejected under 35 U.S.C. 102(e) as being anticipated by Li et al. (USPAP 2003/0189202).

11. Li et al. teach an electronic substrate (10) having a plurality of semiconductor devices (12), comprising a substrate, a thin film of nanowires (34), formed on said substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions, and contacts (18) formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor device. A subset of the

semiconductor device comprises an active matrix driving circuit (paragraph 26). The semiconductor device comprises interconnects between a subset of semiconductor devices (paragraph 25). The substrate comprises a transparent flexible thin film (paragraph 21). The nanowires are doped (paragraph 37). The nanowires are aligned (paragraph 36). The semiconductor device further comprising a layer of oxide (36) deposited on a portion of the nanowires (paragraph 44).

12. Claims 173, 175, 177, 190, 191, 209 – 213 are rejected under 35 U.S.C. 102(b) as being anticipated by Russell et al. (US Patent 5962863).

13. Russell et al. teach an electronic substrate having a plurality of semiconductor devices including light-emitting diodes (col. 1 lines 40 – 45, & col. 2 lines 42 – 47), comprising a substrate (150), a thin film of nanowires (140), formed on said substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions, and anode and cathode (230) formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor device. The substrate comprises a transparent material (abstract). A subset of the semiconductor device comprises an active matrix driving circuit (paragraph 26). The nanowires are single crystal nanowires with mobility comparable to that of electric carries in traditional planar single crystal semiconductor material (col. 6 line 37 – col. 7 line 7). The nanowires are patterned (col. 4 line 66 – col. 5 line 52).

14. Claims 173, 218, and 221 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuekes et al. (US Patent 6256767).

15. Kuekes et al. teach an electronic substrate having a plurality of semiconductor devices, comprising a substrate, a thin film of nanowires of randomly oriented, formed on the substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions, and contacts formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor device (col. 7 lines 47 – 67).

16. The limitations:

wherein said patterned nanowires are photolithography patterned;

wherein said patterned nanowires are screen printed;

wherein said patterned nanowires are ink jet printed;

wherein said patterned nanowires are micro-contact printed;

wherein the nanowires are spin casted;

wherein the nanowires are mechanically aligned;

wherein the nanowires are flow-aligned;

wherein the nanowires are spin casted; and

wherein the nanowires are shear-force aligned; have not been considered. The method of forming a device is not germane to the issue of patentability of the device itself.

17. Prior art considered, but not used in the rejection include Lieber et al. (USPAP 2003/0089899).

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2825

IA

September 25, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800